

# SSI2162

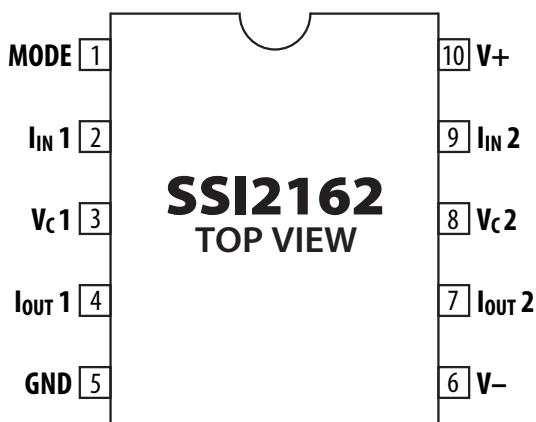
## FATKEYS™ DUAL VOLTAGE CONTROLLED AMPLIFIER

The SSI2162 is a versatile VCA building block for high-performance audio applications. Two independent channels provide voltage control of a current-mode input and output for a gain range from +20dB to -100dB, with control provided by a ground-referenced -33mV/dB constant.

The device offers considerable flexibility for a wide range of design goals and applications. A unique mode control allows selection of Class A, Class AB, or in-between using a single resistor. In addition, improved current handling allows use of lower value input resistors for reduced output noise without loss of headroom. Both channels can be parallel-connected for further noise improvement. Finally, SSI2162 VCA channels can be used as high-quality OTA building blocks for a variety of applications such as voltage controlled filters, exponential generators, and antilog converters.

The SSI2162 will operate on supplies as low as +8V for battery-powered devices such as guitar pedals, or up to  $\pm 18V$  in systems where maximum headroom is desired.

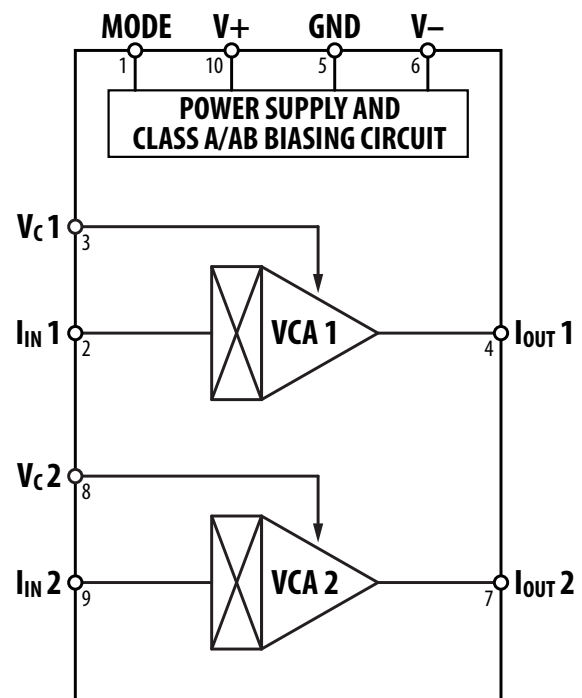
The SSI2162 is part of a family of affordable high-performance VCA's from Sound Semiconductor. The SSI2164 offers four VCA's in a compact SOP package with lowest cost-per VCA, and the single-channel SSI2161 provides lowest noise.



**PIN CONNECTIONS**  
10-LEAD SSOP

### FEATURES

- Two High-Performance VCA's in a Single Package
- Pin-Selectable Class A or AB Operation
- 3dB Lower Noise than SSI2164
- 123dB Dynamic Range (Class AB)
- Low Distortion – Typical 0.025% (Class A)
- Large Gain Range: -100dB to +20dB
- Ultra-Compact 10-Lead SSOP Package
- $\pm 4V$  to  $\pm 18V$  Operation
- No External Trimming
- Low Control Feedthrough – Typically -60dB



**FUNCTIONAL BLOCK DIAGRAM**

**SPECIFICATIONS** ( $V_S = \pm 15V$ ,  $V_{IN} = 0.775V_{RMS}$ ,  $f = 1kHz$ ,  $A_V = 0dB$ , Class AB,  $T_A = 25^\circ C$ ; using Figure 1 circuit without diode)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>POWER SUPPLY</b>						
Supply Voltage Range	$V_S$		$\pm 4$		$\pm 18$	V
Supply Current	$I_S$	Class AB, $V_C = GND$		$\pm 6$	$\pm 8$	mA
Supply Current	$I_S$	Class A, $V_C = GND$ , $I_M = 1mA$		$\pm 8.0$		mA
Power Supply Rejection Ratio	PSRR	60Hz		90		dB
<b>CONTROL PORTS</b>						
Input Impedance			4.5	5	5.5	k $\Omega$
Gain Constant		After 60 seconds of operation		-33		mV/dB
Gain Constant Temp. Coefficient				-3300		ppm/ $^\circ C$
Control Feedthrough		$A_V = 0dB$ to $-40dB$		-60		dB
Gain Accuracy		$A_V = 0dB$		$\pm 0.30$		dB
		$A_V = +20dB$		$\pm 0.55$		dB
		$A_V = -20dB$		$\pm 0.55$		dB
Channel-to-Channel Gain Matching		$A_V = 0dB$		0.07		dB
		$A_V = -40dB$		0.24		dB
Maximum Attenuation				-100		dB
Maximum Gain				+20		dB
<b>SIGNAL INPUTS</b>						
Input Bias Current	$I_B$			$\pm 10$		nA
Input Current Handling				1.9		mA <sub>P</sub>
<b>SIGNAL OUTPUTS</b>						
Output Offset Current		$V_{IN} = GND$		$\pm 150$		nA
Output Compliance				$\pm 100$		mV
<b>PERFORMANCE</b>						
Output Noise		Class AB (20Hz -20kHz, unweighted)				
		$R_{IN/OUT} = 15k\Omega$		-96		dBu
		$R_{IN/OUT} = 10k\Omega$		-99		dBu
		$R_{IN/OUT} = 7.5k\Omega$		-101		dBu
		$R_{IN/OUT} = 3.74k\Omega$		-105		dBu
		Class A (20Hz -20kHz, unweighted) <sup>1</sup>				
		$R_{IN/OUT} = 15k\Omega$		-84		dBu
		$R_{IN/OUT} = 10k\Omega$		-88		dBu
		$R_{IN/OUT} = 7.5k\Omega$		-90		dBu
		$R_{IN/OUT} = 3.74k\Omega$		-96		dBu
Headroom	HR	1% THD		+22		dBu
Total Harmonic Distortion	THD	Class AB (80kHz BW)				
		$A_V = 0dB$		0.05		%
		$A_V = 0dB$ , $V_{IN} = -17dBu$		0.025		%
		$A_V = +20dB$		0.20		%
		$A_V = -20dB$		0.045		%
		Class A (80kHz BW) <sup>1</sup>				
		$A_V = 0dB$		0.025		%
		$A_V = 0dB$ , $V_{IN} = -5dBu$		0.015		%
		$A_V = +20dB$		0.17		%
		$A_V = -20dB$		0.025		%
Channel Separation		$C_F = 10pF$		-110		dB
Unity Gain Bandwidth		$C_F = 10pF$		500		kHz
Slew Rate	SR			700		$\mu A/\mu s$

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage	$\pm 20V$
Storage Temperature Range	$-65^\circ C$ to $+150^\circ C$
Operating Temperature Range	$-40^\circ C$ to $+85^\circ C$
Lead Temperature (Soldering, 10 sec)	$260^\circ C$
Mode Current ( $I_M$ ; Pin 1 to Pin 10 via $R_M$ )	2.0mA
Control Pin Voltage (Pins 3, 8)	V- to V+

**ORDERING INFORMATION**

Part Number	Package Type	Quantity
SSI2162SS-TU	10-Lead SSOP* - Tube	100
SSI2162SS-RT	10-Lead SSOP* - Tape and Reel	4000

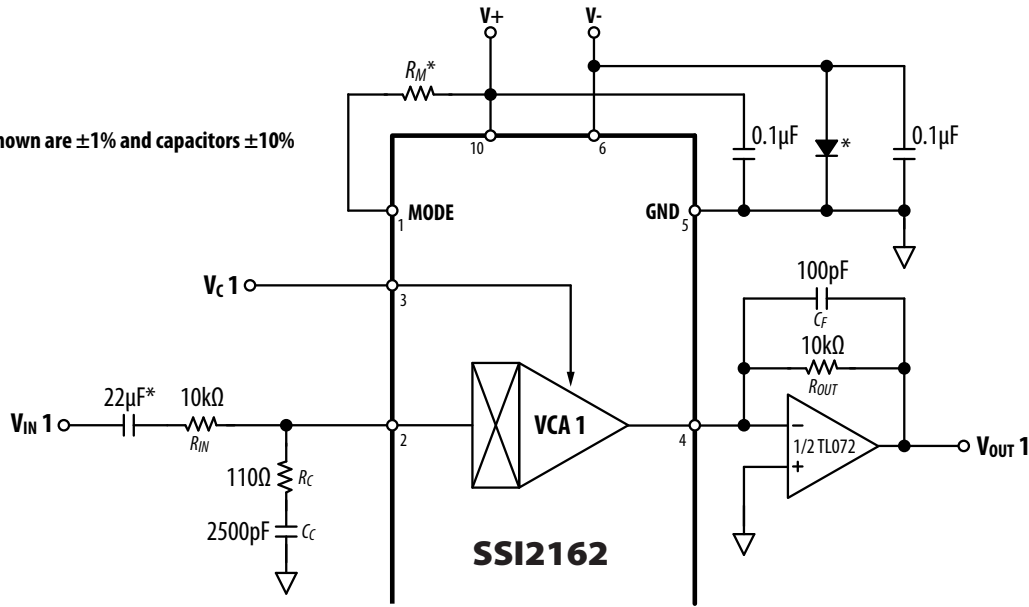
\*SSI Package ID "PSSL10"; mechanical drawing available at [www.sound-semiconductor.com](http://www.sound-semiconductor.com)

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**NOTES:**

All resistors shown are ±1% and capacitors ±10%

\*See text



**Figure 1: Typical Application Circuit**

**USING THE SSI2162**

The SSI2162 is a two-channel voltage controlled amplifier with a control range from +20dB to -100dB. Each VCA is an independent current-in, current-out device with a separate voltage control port. Only the mode control affects both channels; otherwise designers have great latitude on use of each channel for a given application. Basic operation is described below; see the “Principles of Operation” section for further details on inner workings of the device and an application section that follows.

**Inputs**

Figure 1 shows the basic application circuit for one channel. A resistor converts the input voltage to an input current, and a 110Ω resistor in series with a 2200pF capacitor connected to ground ensures stable operation. The SSI2162 is quite tolerant of RC network selection, but 110Ω/2200pF has been proven to work well over a wide range of R<sub>IN</sub> values. If desired, compensation can be calculated as follows:

$$R_C = 0.025 \times R_{IN} \quad C_C = \frac{10^{-5}}{R_{IN}}$$

A 10kΩ value for R<sub>IN</sub> is recommended for most applications, but can range from 3.75kΩ to 100kΩ – lower values will produce the best noise performance at some cost in distortion.

Maximum input current handling is approximately 2mA peak. This input current “headroom” is only likely to be a consideration when using R<sub>IN</sub> values of 10kΩ and below with supplies of ±12V and higher. In such cases, one may want to design the signal chain for a maximum input current of 1.8mA to allow adequate headroom.

An optional series-connected 22µF capacitor is recommended for improved control feedthrough.

**Signal Outputs**

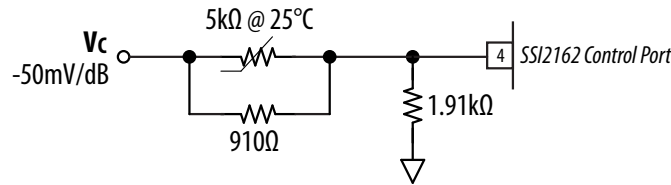
The output current pin should be maintained at virtual ground using an external amplifier such as a TL072; feedback shown results in unity gain. Many op-amps require a feedback capacitor to preserve phase margin. A value of 100pF will suffice in most cases; larger values can be used to reduce high-frequency noise at the expense of bandwidth. In most cases, headroom will be limited by the op amp – increased headroom can be achieved by using a rail-to-rail amplifier or operating on separate supplies.

**Control Ports**

The SSI2162 provides exponential control with gain constant of -33mV/dB; to realize the full gain range of +20dB to -100dB, control voltage should span from -660mV to 3.3V, respectively. If only attenuation is desired, the control port can be driven directly from a low impedance voltage-output DAC.

The control input has a nominal impedance of 5kΩ, with an internal 10:1 resistor divider. Because of this, any resistance in series with V<sub>C</sub> will attenuate the control signal somewhat. If precise control of gain and attenuation is required, buffering the control voltage is suggested.

The 33mV/dB control voltage law is essentially set by transistor physics, and has the property of being proportional to absolute temperature, or approximately 0.33%/°C. This is low enough to be unimportant in most applications, but can be reduced with external temperature-dependent networks. One example is shown in Figure 2 using an inexpensive NTC thermistor (such as Vishay NTCLE100E3502JB0 or similar).

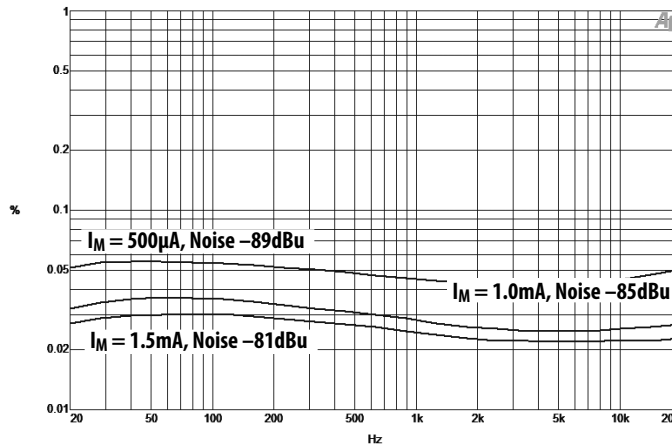


**Figure 2: Temperature-Compensated Control Port**

**Class A Mode Current**

The SSI2162’s gain core can be biased as Class A, AB, or in-between. Class AB will yield the best noise performance which is achieved with Pin 1 left open. Class A offers lowest distortion and requires connection of resistor  $R_M$  between Pin 1 and  $V_+$ .

As Figure 3 shows, mode current  $I_M$  affects both noise and distortion. For most applications, a 1mA mode current provides the best overall Class A performance. One can reduce THD further by increasing mode current, but at a significant cost in noise. In addition, increased mode



**Figure 3: SSI2162 Class A THD+N At Varying Mode Currents**  
 $R_{IN} = 10k\Omega, V_{IN} = 0dBu, A_V = 0, V_S = \pm 15V, 22Hz - 80kHz$  Filter

current increases supply current. For example, supply current is typically  $\pm 8.4mA$  with a 1.0mA mode current, but jumps to nearly  $\pm 11mA$  at 1.5mA. Under no circumstances should mode current exceed 2mA. For some applications, the designer might consider mode current below 1mA for improved Class A noise and power dissipation.

Resistor  $R_M$  can be calculated by:

$$R_M = \frac{+V - 0.65V}{I_M}$$

See the “Principles of Operation” section for further discussion on gain core biasing.

**Unused Channels**

If either channel of the SSI2162 is unused, the input and output should be grounded and control pin left open or grounded. Rather than put a channel to waste, however, the designer might consider ways to put it to use for additional functionality, or parallel with another channel for reduced noise.

**Supplies**

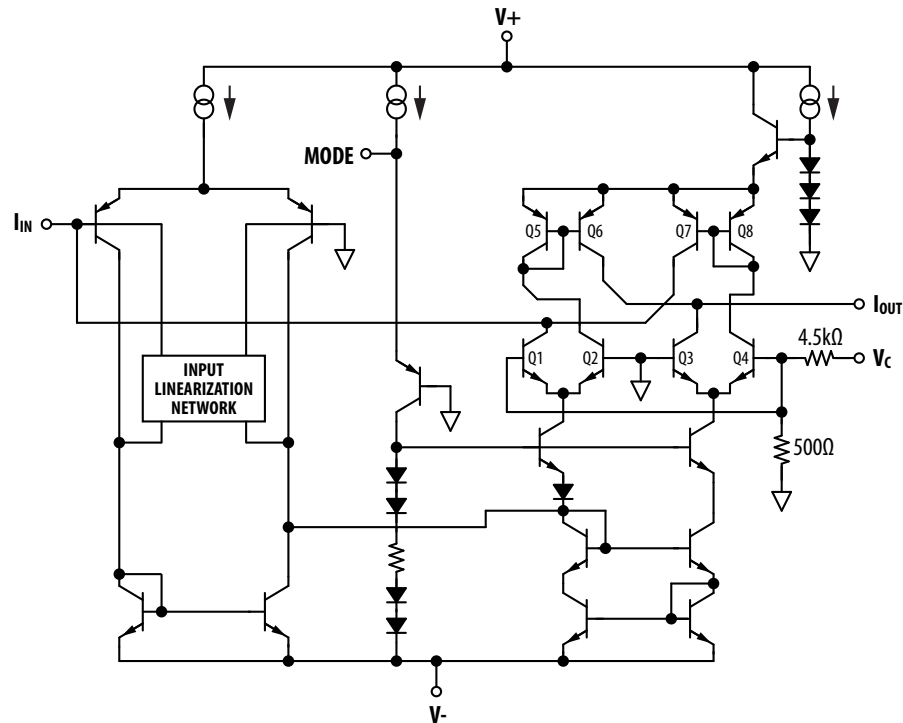
Supplies from  $\pm 4V$  to  $\pm 18V$  are possible, which should be regulated and include normal design practices such as bypass capacitors as shown in Figure 1. Since internal protections were added to prevent catastrophic failure that may be experienced during SSM/V2164 asymmetrical

power-up, the typical Schottky diode solution is no longer necessary. In most applications, no diode is needed. Modular synthesizer sub-systems may want to include a standard 1N4148-style diode as an extra measure of protection since “hot” plugging of modules may be experienced.

Single supply operation is described in the Applications section.

## PRINCIPLES OF OPERATION

### VCA Core



**Figure 4: SSI2162 Simplified Schematic**

The simplified schematic in Figure 4 shows the basic structure of a VCA cell. The gain core is comprised of matched differential pairs Q1 – Q4 and current mirrors Q5, Q6 and Q7, Q8. The current input pin,  $I_{IN}$ , is connected to the collectors of Q1 and Q7 and the difference in current between these two transistors is equivalent to  $I_{IN}$ . For example, if 100  $\mu$ A is flowing into the input, Q1’s collector current will be 100  $\mu$ A higher than Q7’s collector current.

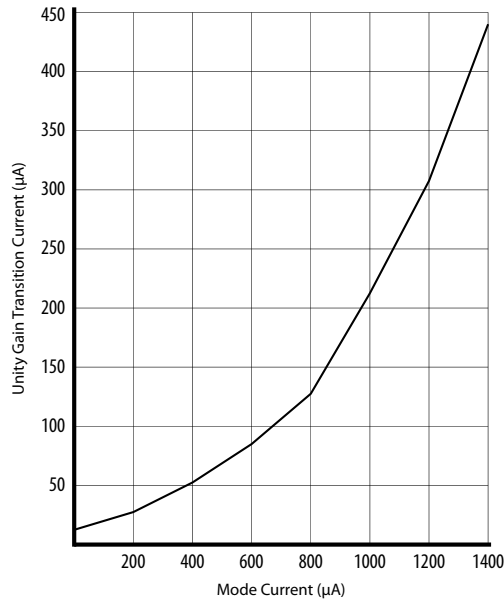
The control voltage  $V_C$  steers the signal current from one side of each differential pair to the other, resulting in either gain or attenuation. For example, a positive voltage on  $V_C$  steers more current through Q1 and Q4 and decreases the current in Q2 and Q3. The current output pin,  $I_{OUT}$ , is connected to the collector of Q3 and the current mirror (Q6) from Q2. With less current flowing through these two transistors, less current is available at the output. Thus, a positive  $V_C$  attenuates the input and a negative  $V_C$  amplifies the input. The VCA has unity gain for a control voltage of 0.0 V where the signal current is divided equally between the gain core differential pairs.

### Biasing the VCA Core

VCA’s operate by modulating differential currents in a transistor core, a fraction of which is steered to the output in a value set by the control voltage. Such VCA’s are generally classified as Class A, Class B and Class AB; terms borrowed from radio transmitter jargon.

In Class A operation the quiescent current in the transistor core is designed to be greater than the maximum input current, so all the transistors remain active at all signal levels. This type of operation produces the lowest distortion, but the high quiescent current level has a severe impact on noise floor and control feedthrough rejection.

In Class B operation the core transistor current is zero and only half the transistors conduct signal at any point of time. Such operation would yield the lowest possible noise floor and near perfect control rejection, but is unfortunately impractical in practice. This is because the transistors effectively disconnect feedback inside the VCA during zero-crossings and low signal levels, potentially causing latch-up or instability. The solution is to arrange the circuit to operate in class A at low signal levels and enter Class B at larger ones. This is known as Class AB operation.



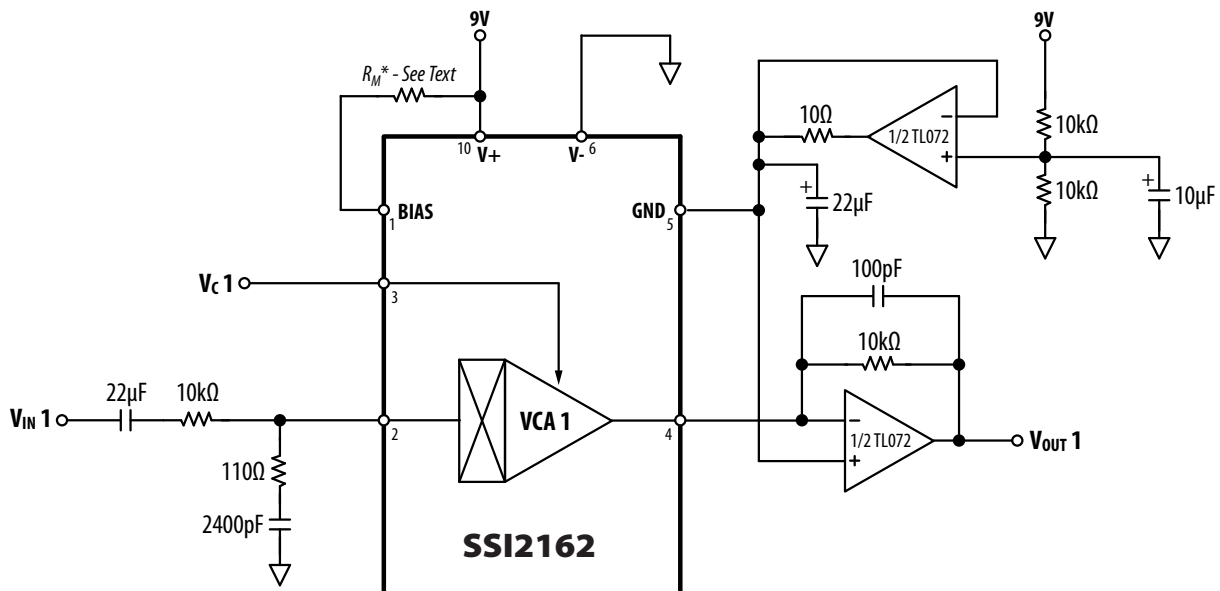
**Figure 5: Class A Mode Current to Transition Current Association**

In some applications, distortion may be more important than noise or control feedthrough, in which case it is desirable to raise the point at which the transition from class A to class B takes place. This can be affected by injecting current into the mode pin. The relationship between the input current transition point and the current injected into the mode pin is intentionally non-linear. Figure 5 shows the relationship between the two.

For example, supposing the desired transition point is at a peak input voltage of one volt. With a 10kΩ input resistor this would correspond to an input current of 100µA, and extrapolating from Figure 5 would require a current of about 650µA to be injected into the mode pin. The mode pin is biased about 0.65V above ground, so a resistor placed between this pin and V+ would see a voltage of 14.35V with a +15V supply. Therefore a resistor value of 22kΩ would work well.

**APPLICATION INFORMATION**

Please refer to the SSI2164 data sheet and AN701 “Designing Voltage Controlled Filters for Synthesizers with the SSI2164” for comprehensive information that is directly applicable to the SSI2162. Be careful to adjust  $R_{IN/OUT}$  as well as the  $R_C$  and  $C_C$  compensation network to recommended SSI2162 values.



**Figure 6: Single-Supply Operation**

**SINGLE SUPPLY OPERATION**

By referencing to a pseudo-ground point midway between V+ and V-, the SSI2162 can operate from a single supply between +8V and +36V. An op amp provides a low-impedance reference, from which all ground connections are made.

As shown in Figure 6, a voltage divider comprised of two 10kΩ resistors connected to the non-inverting input provides a ground voltage reference, the output of which is connected to ground on the SSI2162. The SSI2162's inputs can be referenced to the same ground, or AC coupled as shown in Figure 6. The 10Ω resistor and 22μF capacitor filter noise that may otherwise be present in the pseudo-ground. Control ports provide unity gain when V<sub>C</sub> is equal to the ground reference voltage, or 4.5V in the case of Figure 6.

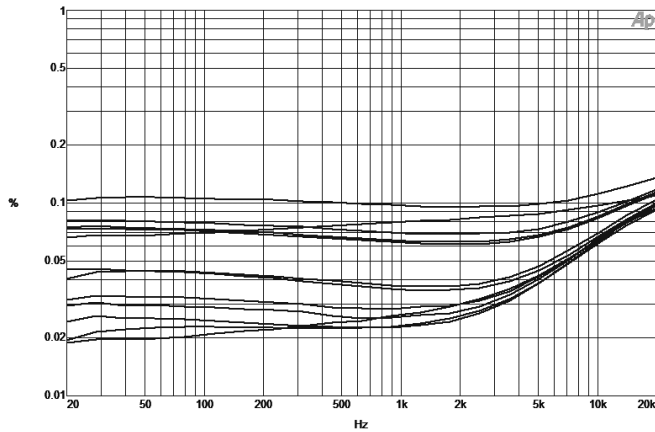
To bias SSI2162 gain cores as class A, the mode resistor value calculation is modified slightly to:

$$R_M = \frac{\frac{+V}{2} - 0.65V}{I_M}$$

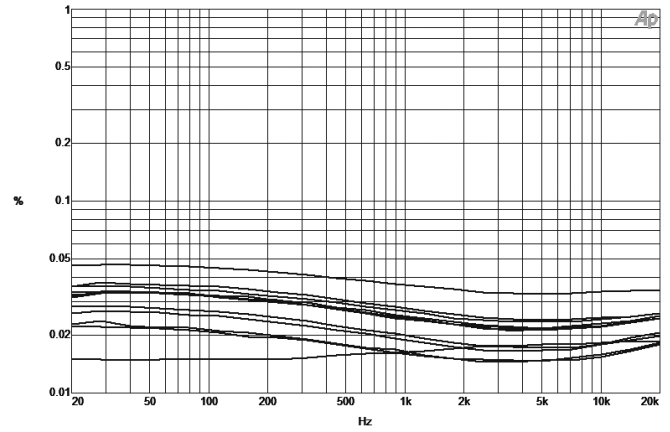
For example, if using 9V supplies R<sub>M</sub> should be 3.9kΩ.

**TYPICAL PERFORMANCE GRAPHS\***

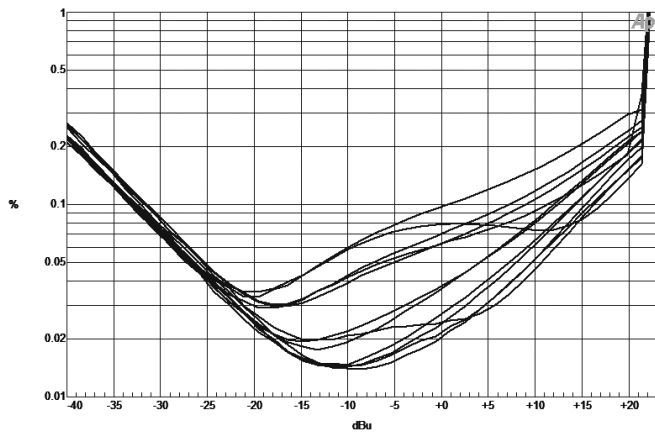
Figure 1 Application Circuit at V<sub>S</sub> = ±15V, A<sub>V</sub> = 0dB, V<sub>IN</sub> = 0dBu, R<sub>IN/OUT</sub> = 10kΩ, f = 1kHz; unless otherwise noted



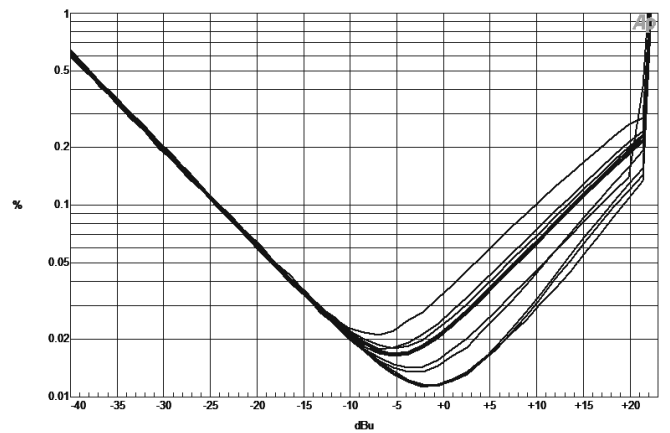
**THD+N vs. Frequency Distribution - 12 Channels**  
*Class AB, 22Hz - 80kHz Filter*



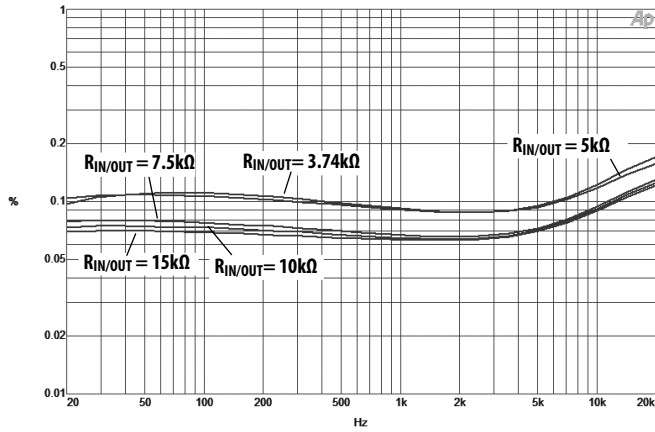
**THD+N vs. Frequency Distribution - 12 Channels**  
*Class A, 22Hz - 80kHz Filter*



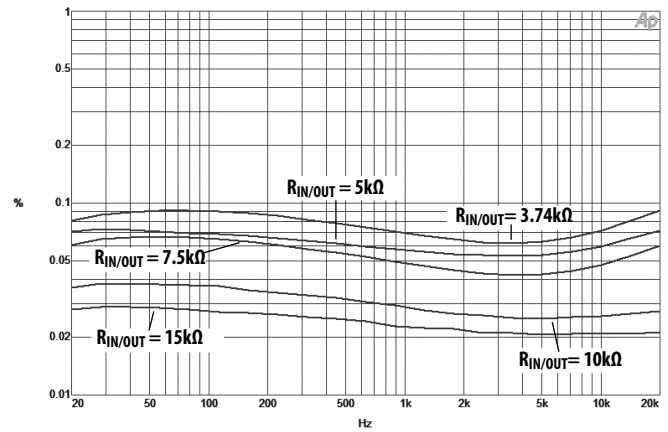
**THD+N vs. Amplitude Distribution - 12 Channels**  
*Class AB, <10Hz - 22kHz Filter*



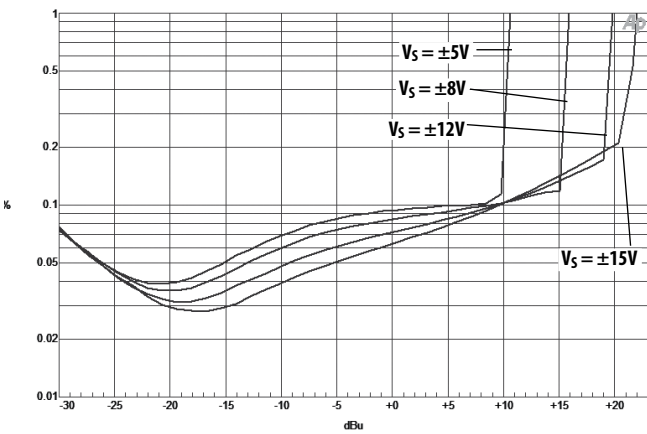
**THD+N vs. Amplitude Distribution - 12 Channels**  
*Class A, <10Hz - 22kHz Filter*



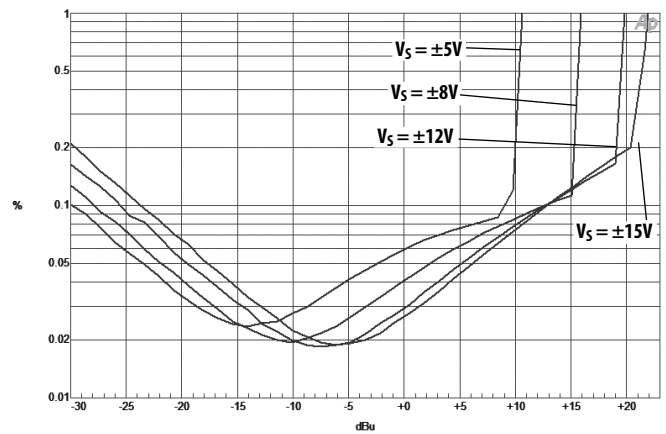
**THD+N vs. Frequency vs.  $R_{IN/OUT}$**   
Class AB, 22Hz - 80kHz Filter



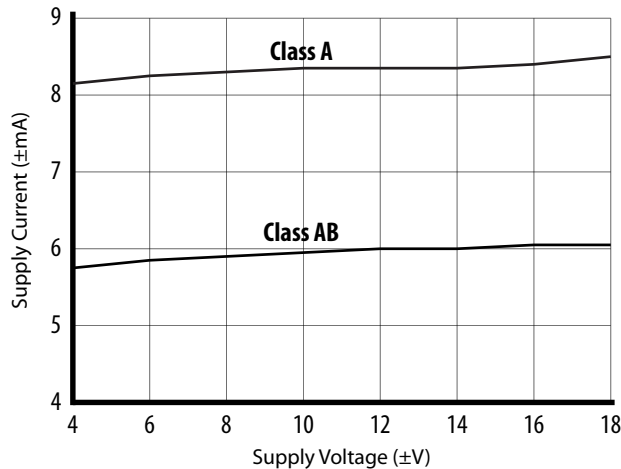
**THD+N vs. Frequency vs.  $R_{IN/OUT}$**   
Class A, 22Hz - 80kHz Filter



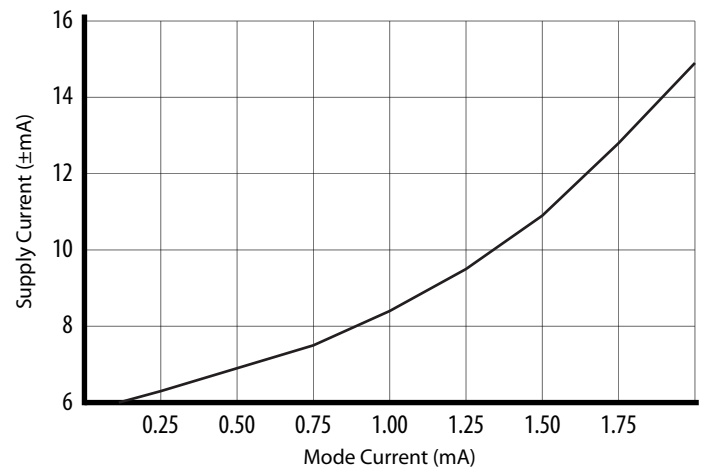
**THD+N vs. Amplitude vs. Supply Voltage**  
Class AB, <10Hz - 22kHz Filter



**THD+N vs. Amplitude vs. Supply Voltage**  
Class A, <10Hz - 22kHz Filter



**Supply Current vs. Supply Voltage**



**Supply Current vs. Mode Current**

**\*About THD+Noise data.** As the name implies, THD+N measures total harmonic distortion *and* noise. In all cases, THD *without* noise will be lower than shown. The noise component will increasingly dominate graph data as signal levels decrease, for example, in THD+N vs. Amplitude graphs. Similarly, an otherwise “apples to apples” comparison between two lines under different noise conditions such as Class A vs. Class AB or differing  $R_{IN}$  values may be affected. While one might dismiss the value of THD+N noise measurements, recall that both distortion and noise are undesirable so such information therefore shows all the things you *don't* want, which may be very useful when setting design limits.